On-Wafer Small-Signal and Large-Signal Measurements up to Sub-THz Frequencies

Invited Paper

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***Abstract* — Recent advances in MMIC technology have opened the possibilities for circuit operation in the THz range. There are numerous examples of BiCMOS and III-V compound device technologies with demonstrated performance beyond 600 GHz. Characterization of such MMIC are predominantly performed on-wafer in a planar environment. However, on-wafer characterization facilities do not fully keep pace with MMIC development in terms of frequency and power. The paper discusses issues involved in on-wafer calibration at mm-wave frequencies, which is the basis for accurate measurements and characterization of active and passive device. Subsequently, the paper discusses mm-wave interconnect characterization. Low-loss interconnects are important for mm-wave MMIC, especially in case of heterogeneous integration. Finally, a novel heterogeneous integration approach of bipolar technologies, using both BiCMOS and InP DHBT processes is presented. This approach heavily relies on low-loss interconnects and accurate device modelling. It will be shown that accurate large-signal models can be efficiently extracted from well-calibrated on-wafer multi-bias small-signal measurements, but verification is difficult due to calibration difficulties at mm-wave frequencies.**

Keywords* — *on-wafer calibration techniques, on-wafer characterization, mm-wave and sub-mm-wave circuits, calibration methodologies, sub-mm-wave transmission lines, interconnects

I. INTRODUCTION

Recent advances in MMIC technology have opened the possibilities for integrated circuit operation in the THz range. There are numerous examples of BiCMOS and III-V compound device technologies, with demonstrated performance beyond 600 GHz. The design of such MMIC is generally based on a detailed knowledge of EM effects of the passives and interconnects, and on good large-signal and small-signal device modelling. Characterization of such MMIC is predominantly performed on-wafer in a planar environment and requires accurate calibration techniques.

But on-wafer characterization facilities do not fully keep pace with MMIC development in terms of frequency of operation and power. Especially critical is the accurate characterization and modelling of devices operational up to THz frequencies. This owes to the fact that accurate on-wafer calibration is difficult at higher frequencies, due to excitation of higher order modes, signal coupling and a multi-mode operation as well as coupling effects corrupting the calibration data. The situation becomes even more difficult with the newly implemented processes utilizing transfer substrates and heterogeneous integration, which exhibit many transitions to a multitude of transmission line technologies. Characterization of passives like interconnects requires calibration up to THz frequencies, while device model extraction necessitates measurements at somewhat lower frequencies. An example, the attenuation of a coplanar waveguide (CPW) line is presented in Fig. 1 as a function of frequency. It shows that corrupted or inaccurate data obtained during calibration leads to inaccuracies in the device under test (DUT) measurement results. The paper will show below that the origin of these issues have to be determined and overcome in order to accurately determine the DUT performance at THz frequencies.

Of particular importance is the choice of the transmission line technologies (e.g. CPW, standard, thin-film and inverted microstrip) and the according interconnects. In particular, the paper discusses transmission line and interconnect performances, using simulations verified with experiments at millimeter-wave frequencies. It is shown that thin-film microstrip or stripline lines are especially suitable for line calibration standards and interconnects at THz frequencies. Further, the paper shows that although active device modelling generally utilize data up to 60 GHz, device model verification requires measurements up to THz frequencies due to the high cut-off and maximum oscillation frequencies of modern bipolar devices. One important aspect for useful

measurements is the control of output power, which has to be sufficiently low for transistor characterization and hence limits considerably the dynamic range of today's measurement equipment. Another aspect is the positioning accuracy of the probes at high frequencies.

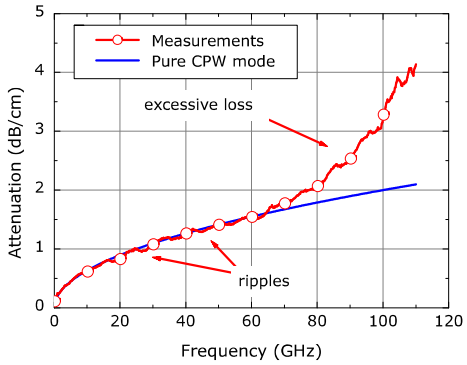

Fig. 1: CPW attenuation versus frequency for a CPW line extracted from measurements using multi-line TRL. The theoretical CPW attenuation is also indicated [3].

Thin-film transmission lines and interconnects are built on top of a substantial dielectric stack on top of the active device layers. In this paper we go a step further and demonstrate that such stacks can be efficiently combined using BiCMOS and III-V technologies at mm-wave frequencies. The paper will demonstrate interconnect and device characterization in this wafer-level heterogeneous integration processes. It is based on a newly established InP-on-BiCMOS process, available now through the SciFab IHP foundry. The transitions from the BiCMOS circuits to the InP circuits and vice versa as well as active device performance will be discussed in detail using simulated and measured results.

II. Pitfalls in On-Wafer Calibration at MM-Wave Frequencies

It becomes indispensable to perform accurate on-wafer device characterization at mm-wave frequencies, due to the increasing transit and maximum oscillation frequencies of the devices employed in such circuits. Generally, results rely to date on extrapolations from low-frequency measurements. The difficulties in on-wafer measurements have many sources, such as for example: crosstalk between probes, crosstalk with other structures on-wafer, parasitic mode excitation with probes, on-wafer calibration errors, probe misalignment, multi-mode propagation on the calibration standards, signal losses, limited dynamic range of equipment due to low signal levels, radiation into the substrate, parallel plate mode excitation in CPW structures etc. Another difficulty appearing at frequencies above 110 GHz is the necessity for re-calibration of the system at each band with the according re-occurrence of all the above difficulties.

The key components for understanding the above effects are the on-wafer probes, the transmission line properties and the calibration procedures employed. Calibration procedures will be treated in the following section, while the other two will be discussed below.

The impact of the on-wafer probe can be understood by considering that the outer structure dimensions are large compared to the on-wafer calibration standard dimensions. This enables the excitation of additional propagating modes on-wafer, which are not related to the desired CPW mode. Firstly, the coupling between probe ground and on-wafer ground creates a parasitic propagating signal. Secondly, in the vicinity of the pad structure a mode is excited similar to the parallel-plate mode between the CPW ground contacts and backside contact. Finally, there is a mode which is guided between the ground of the coaxial probe and the wafer backside metallization. Fig. 2 shows these effects obtained from 3D EM simulations of calibration standards employing microstrip lines. The interaction of the probe with the surrounding structures is clearly visible.

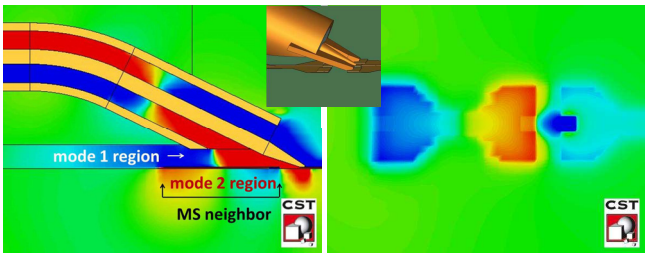

Fig. 2: Left: Electrical field E_y in the longitudinal cross-section (y is the vertical axis, blue color means negative, red color positive and green color zero field values, respectively); Right: Electrical field E_y in the top view cross section directly under the ground metallization of the microstrip lines (y is the normal direction). Inset: The exciting probe positioned over a short neighboring microstrip line [3].

The impact of this coupling and excitation of parasitic modes on the calibration procedure can be evaluated, when simulating different calibration standards in microstrip technology [4] and CPW environment [1], [2], [5], [6], respectively. As an example, Fig. 3, shows simulated results for S_{21} of three different transmission line lengths, which are typically used during calibration. It can be concluded from the figure that coupling to a neighboring line gives rise to transmission dips at frequencies related to the length of this line. Coupling to several lines on both ends of the DUT will give rise to several dips in the frequency characteristic. These dips are then responsible for measurement inaccuracies in the final measurements after calibration, independent of the calibration methodology used.

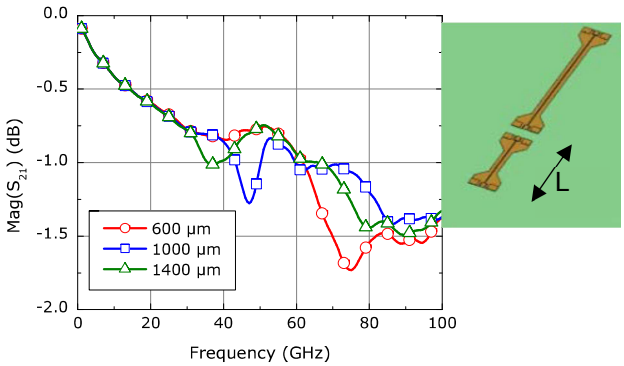

Fig. 3: Signal transmission for neighboring short microstrip lines of three different lengths (L = 600 µm, 1000 µm and 1400 µm) corresponding to pronounced resonance points (75, 48 and 37 GHz) [4].

It is common practice to employ CPW waveguides as calibration standards on-wafer in addition to the calibration substrates. These calibration standards are prone to parallel-plate mode propagation and consequently to substrate mode excitation. Fig. 4 illustrates the coupling effect for a substrate placed on top of a ceramic mimicking an infinite substrate and the same situation with a metallized back-plane. One can clearly see the strong coupling into a parallel-plate mode in case of backside metallization.

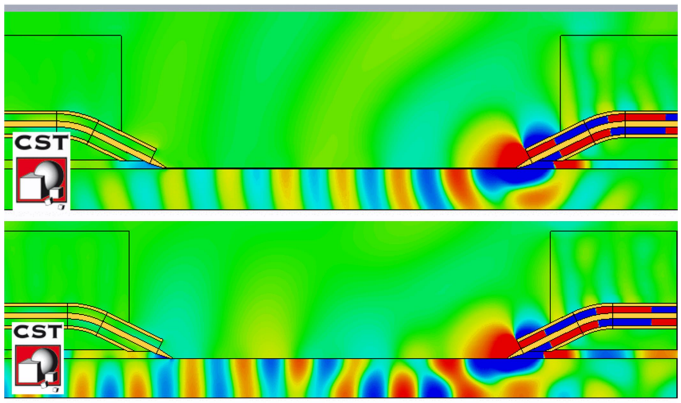

Fig. 4: Field plots from CST Microwave Studio simulations with the CPW substrate placed on: ceramic (top) and metal (bottom). Open boundary condition is applied at the bottom for ceramic CPW substrate, while an electric wall boundary is applied for metal CPW substrate [22].

III. Advanced Calibration Procedures

A. On-Wafer Calibration

Scattering (S)-parameter measurements of devices fabricated on semiconductor wafers are usually calibrated using a two-step procedure: first the measurement reference plane is set close to the RF probe tips using suitable calibration substrates and then parallel and serial parasitic impedances are characterized by measurements of the device de-embedding elements. As it was demonstrated in [13]–[15], the on-wafer S-parameter calibration with *in-situ* standards is the preferable strategy for accurate device characterization at sub-mm-wave frequencies, in particular on silicon. The measurement reference plane is shifted close to the device terminals (Fig. 5). Application of commercial planar calibration standards assures consistent level of calibration accuracy for the wafer-level S-parameter measurement system [11]. This procedure remains accurate only if the above coupling effects on the calibration substrate can be ignored. In addition, de-embedding of the device back end of line (BEOL) parasitics becomes a challenge at mm-wave and sub-mm-wave frequencies due to the increased complexity of the BEOL equivalent circuit and de-embedding algorithms, involving more than five measurement steps (e.g. [12]).

While a great variety of S-parameter calibration methods are available nowadays, the multiline thru-reflect-line (mTRL) [16] and the transfer thru-match-reflect (TMR, or LRM) [17] are relevant for implementation. The convincing advantage of mTRL is its capability to directly measure the S-parameters of *in-situ* transmission lines at a well-defined single-mode reference plane setting the calibration reference impedance Z_{REF} to the characteristic impedance of the line standard [20], [21]. Thin-film lines provide line standards with characteristic impedance close to 50 Ω and reduced dispersion region using modern semiconductor technologies. Therefore, the transformation of the calibration reference impedance to the system of 50 Ω reference impedance (i.e. to "pseudo S-parameters", [18]) may not be required for the majority of measurement tasks. The remaining practical limitation of the mTRL, however, is the relatively big size of the test chip taken by calibration standards and the need to re-position wafer probes during calibration procedure. It is important to note, that the minimal size of the TRL chip is reverse proportional to measurement frequencies and is less relevant at sub-mm-wave frequencies, omitting low frequencies.

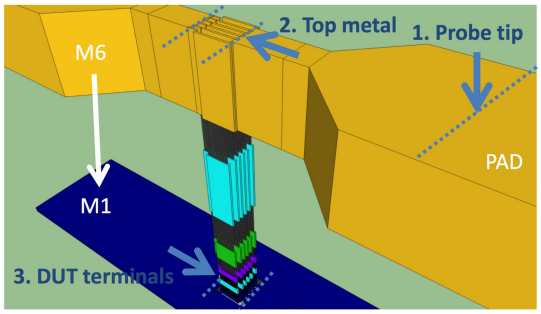

Fig. 5: Three different locations of the reference plane: probe tip, top metal and DUT terminals

The transfer TMR approach has a remarkable advantage: it requires only three standards with the same geometry taking the minimum space of a test chip. The TMR can be easily automated and runs without the need of operator interaction on a conventional wafer probe system. However, the accurate determination of the calibration reference impedance of TMR at sub-mm-wave range is difficult (same holds for any other lumped-standard based calibration method). While [19] suggested several methods applicable for W-band range, the solution for higher frequencies is still underway.

B. Calibration Reference Plane

Designing *in-situ* broadband thin-film transmission lines close to the DUT terminals necessitates the utilization of the top metal level, for instance M6 for the ST Microelectronics' BiCMOS9MMW process (Fig. 6), or the LB metal for IBM's SOI12S0 process (Fig. 7). Therefore, the optimal position of the *in-situ* calibration reference plane is at the top metal level and can be shifted from the top metal to the intrinsic device terminals by a conventional de-embedding approach. Because the parasitic impedance of the contact pads and interconnect lines are already included into the systematic calibration error model, the equivalent impedance of the de-embedding elements should be mostly of pure lumped nature [20], [21].

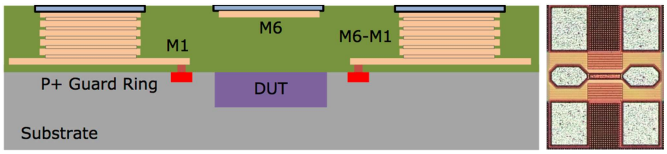

Fig. 6: Cross-section (left) and a photograph (right) of the thru standard implemented in the ST Microelectronics' Si/SiGe:C BiCMOS9MMW process(taken from [20]).

The work in [15] demonstrated an implementation of the *in-situ* mTRL calibration up to 750 GHz frequencies with smooth and consistent propagation constant suitable for transistor device characterization. The calibration lines were realized in a thin-film microstrip design on a thin bisbenzocyclobutene-based (BCB) monomers film. Later, a similar experiment was performed on calibration lines realized by IBM's SOI12SO process (Fig. 8). These results confirm that suitable sub-mm-wave transmission lines for calibration purposes can be realized using thin-film transmission lines and mTRL is applicable.

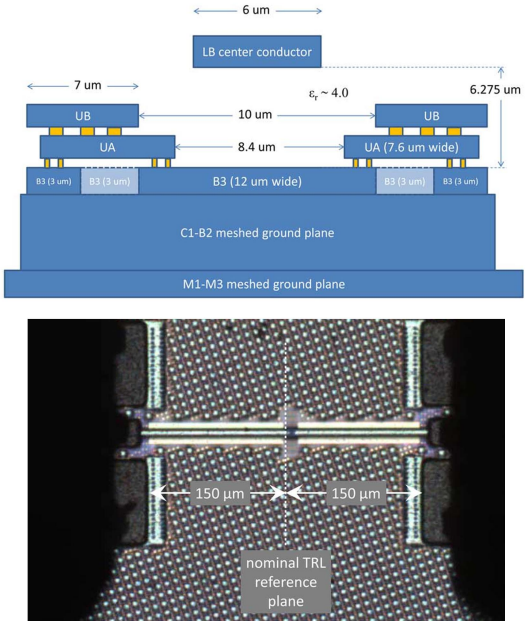

Fig. 7: Cross-section of the transmission-line (top) and test structure (bottom) implemented in IBM 45-nm complementary metal-oxide-semiconductor (CMOS) silicon-on-insulator SOI12S0 integrated-circuit process [21].

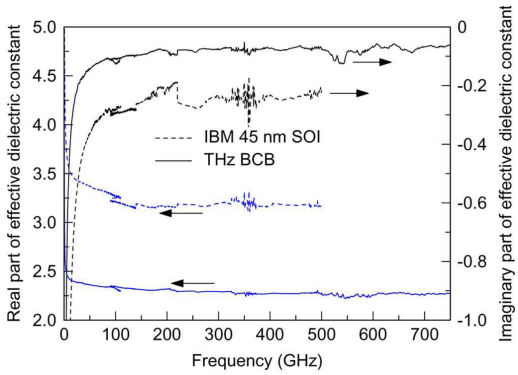

Fig. 8: Comparison of measured effective dielectric constant of the line standard implemented in Teledyne BCB and IBM's SOI process [21]).

C. Correction for Crosstalk and Coupling

With increase of measurement frequency to the sub-THz range, the impact of parasitic effects described above can significantly contribute to the calibration residual errors. Then, the conventional approach of modeling the systematic measurement errors of a wafer probe measurement system by twelve error terms becomes insufficient. A comprehensive study of two different approaches, the 16-term and the two-tier interior crosstalk models was reported recently in [22]. It was demonstrated that correction for the parasitic coupling and crosstalk errors become relevant already at upper W-band frequencies (Fig. 9). Several useful recommendations on optimization of on-wafer standards were given there, such as minimizing of the signal-conductor width and the gap to the ground conductors for CPW standard design and keeping the access lines short.

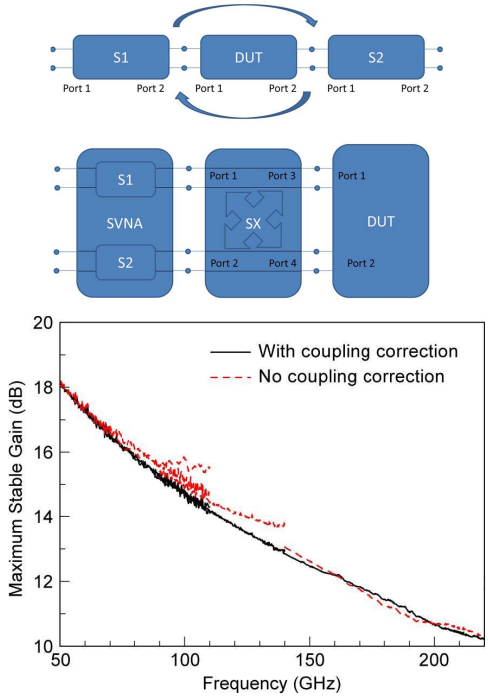

Fig. 9: Two-tier interior crosstalk model (top) and the maximum stable gain of a transistor corrected with standard TRL and with TRL augmented with coupling corrections (bottom) [22].

IV. MM-Wave Device On-Wafer Characterization

A. Interconnects and Transmission Lines

Mm-wave and sub-mm-wave MMIC require low-loss interconnects and low-loss transmission lines. As indicated in the previous section, thin-film and inverted microstrip lines have demonstrated suitability for MMIC applications up to THz frequencies, due to their advantageous characteristics [21].

Thin-film microstrip lines require, however, an appropriate dielectric stack with the according interconnects. Fig. 10 shows a comparison of simulated and measured transmission coefficient up to 220 GHz for a thin-film microstrip line in BiCMOS, with interconnect transitions to a BCB thin-film microstrip line and pads in InP technology. These results confirm the broadband capabilities of low-loss interconnect transitions employed in thin-film transmission line technology. In fact, the losses of each transition from the BCB to the BiCMOS stack are lower than 0.5 dB at 220 GHz. Such low-loss transition structures can be employed in heterogeneous integration, as described below or for chip-to-chip transitions. Measurement results for similar lines are presented in Fig. 11 for different line lengths. These results demonstrate the

usefulness of such lines and interconnects for calibration and circuit purposes.

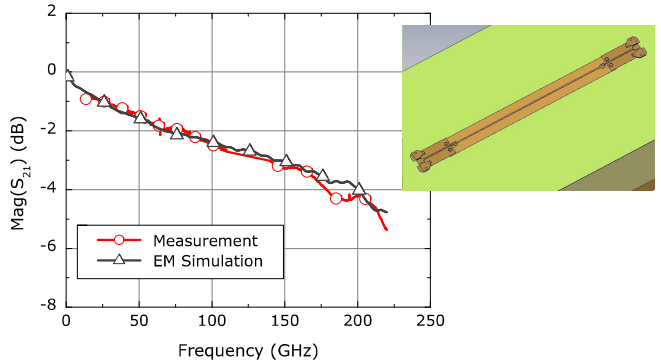

Fig. 10: Comparison of simulated and measured transmission losses of a microstrip line on BiCMOS probed through a microstrip line on InP heterogeneously integrated on top of the BiCMOS wafer. The results include line losses and losses due to two transitions between the two technologies [8].

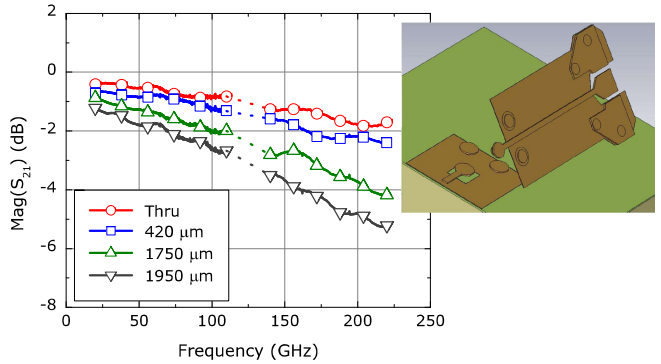

Fig. 11: Comparison of simulated and measured transmission losses of a microstrip line on BiCMOS probed through a microstrip line on InP heterogeneously integrated on top of the BiCMOS wafer. The results include line losses and losses due to two transitions between the two technologies.

Thin-film transmission lines exhibit also a relatively small phase constant as can be seen in Fig. 12 with a respective attenuation constant of around 1 dB/mm at 200 GHz.

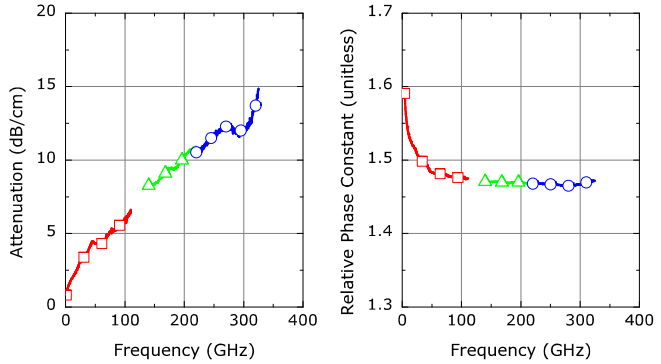

Fig. 12: Measured attenuation constant (left) and relative phase constant (right) frequency characteristics of a thin-film microstrip line in BCB.

B. *Transistor Devices and MMIC*

Wafer-level device characterization technology made a substantial progress in the last decade: RF probe frequency capabilities increased exponentially, new probe technologies came to place and the list of probe manufactures expanded [23]. Recently, micromachined probes designed to facilitate the development of TMICs in the 750 GHz to 1.1 THz frequency range have been introduced. This probe demonstrated an insertion loss of less than 7 dB and a return loss of greater than 15 dB, as can be observed in Fig. 13 [24].

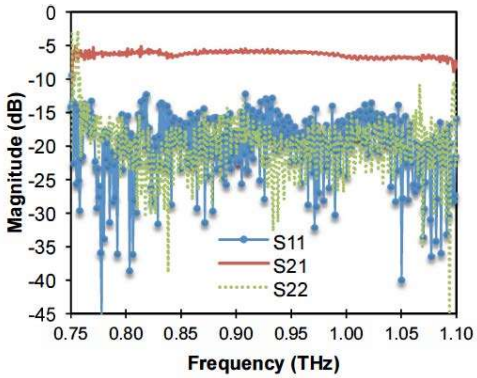

Fig. 13: Measured S-parameters of the 1.1 THz wafer probe [24].

While small-signal measurement capabilities of modern systems have already achieved the THz frequency range, the more sophisticated wafer-level large-signal and noise measurements still remain a great challenge. Load-pull and RF noise measurement systems for the W-band are seldom available. The traditional load-pull techniques that require integration of the electro-mechanical impedance tuners on the wafer probe system suffer from high losses (e.g. larger than 2 dB at W-band) and other limitations at millimeter-wave frequencies and beyond. As a result, the maximum reachable reflection coefficient of such systems is lower than 0.6.

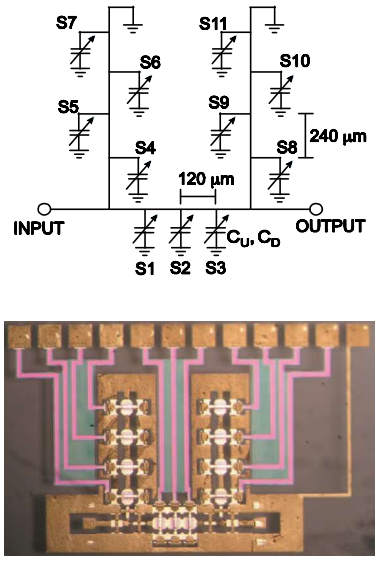

Fig. 14: The schematic diagram (top) and the photograph (bottom) of the W-band double-stub MEMS switch impedance tuner [26].

A novel concept of an active real-time load-pull W-band system with frequency up/down conversion technique was reported in [25]. The authors claimed to reach load reflection coefficients as high as 0.95 at 94 GHz. Nearly full coverage of

the Smith chart enables verification of the large-signal device models and accurate characterization of microwave integrated circuits the sub-THz frequency range. An alternative approach to minimize the setup losses is to integrate a reconfigurable impedance tuner into the wafer probe [26]. The schematic circuit and a micrograph are shown in Fig. 14. Realizing double and triple switching topologies and using MEMS switches, maximum load reflection coefficient lower than 0.92 and 0.82 were achieved for 75 GHz and 100 GHz frequencies, respectively.

A further step toward reducing the setup losses is the integration of the tuner on-wafer, e.g. the *in-situ* impedance tuning. In [27] the design of an *in-situ* impedance tuner and measurement results of the device noise parameters obtained at D-band have been presented. As it was originally discussed in [28], the tuner is based on 50 Ω transmission lines and digital tunable capacitances (DTC) connected in parallel. It can provide 32 different impedance points, optimized for characterization of a particular device, as illustrated in Fig. 15. As it is claimed in [27] the developed *in-situ* impedance tuning technique is an efficient solution for extracting the device noise parameters in the entire D-band range.

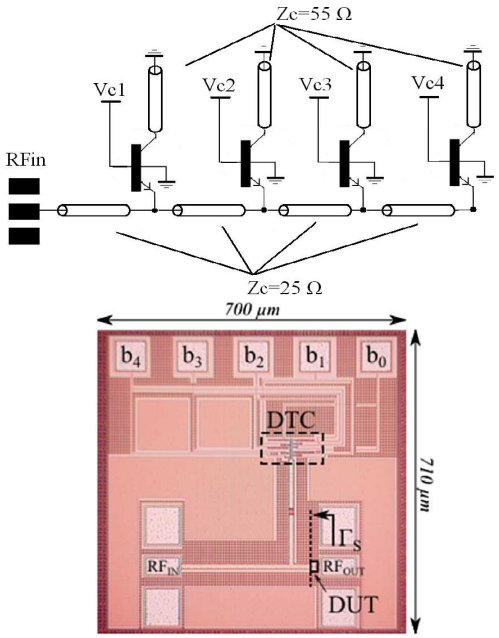

Fig. 15: The schematc of the DTC (top) and a photograph of the D-band source-pull *in-situ* impedance tunners (bottom). Pictures from [27], [28].

C. Large-Signal Device Characterization

The small-signal equivalent circuit parameters for transistor devices in two-terminal and three-terminal configurations are determined by employing a direct parameter extraction methodology. The accuracy of this extraction relies entirely on the accuracy of the on-wafer calibration and on the accuracy of the reference plane shift towards the intrinsic device terminals. Assuming that the calibration issues described above have been avoided and a suitable calibration procedure has been applied allows for direct parameter extraction using multi-bias S-parameter transistor measurements. As an example, results for InP III-V based HBTs are presented here based on [29]. After transferring the elements found from small-signal extraction to the large-signal model, the parameters affecting the DC and thermal characteristics of the device are determined. The large-signal model can accurately predict large-signal performance including device scaling, as illustrated in Fig. 16.

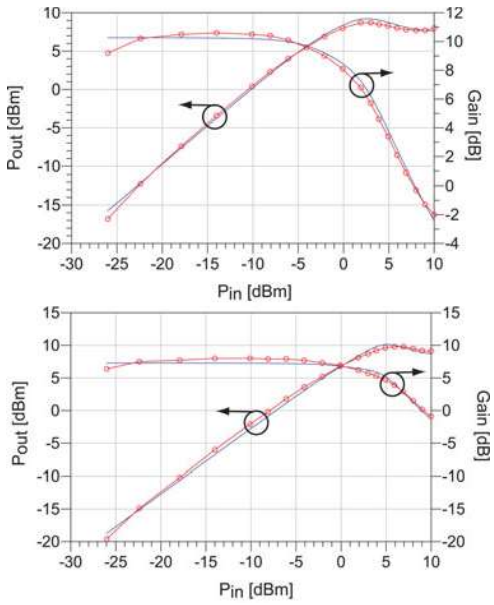

Fig. 16: Measured (solid line w. symbols) and simulated (solid line) large-signal performance at 77 GHz for single-finger device biased at V_{ce} = 1.4 V with a quiescent current of I_{cq} = 22.7 mA (top) and two-finger device biased at V_{ce} = 1.4 V with a quiescent current of I_{cq} = 29.6 mA (bottom) [29].

These results demonstrate a successful sequence of steps comprised of on-wafer system calibration, low-loss interconnect transitions and single mode transmission lines, reference plane shift, small-signal model parameter extraction and finally large-signal parameter extraction. This procedure is subsequently applied to the characterization of devices in the heterogeneous integration technology described below.

V. Heterogeneous MMIC Device Testing

Wafer-level integration of heterogeneous technologies has recently attracted a lot of attention, due to technological developments in several large-scale projects, such as e.g. COSMOS [5], [6], or SciFab [7]–[10]. The major driving force is to provide high-speed III-V semiconductor devices on Si platforms, providing not only speed improvement without trade-off in signal amplitude, but also functional complexity to high-speed circuits.

Such technology developments put high demands on device characterization. Fig. 17 illustrates schematically the cross-section of the InP-on-BiCMOS process. One challenge is the device characterization of devices after heterogeneous wafer-level integration. The characterization of the impact of such a technology on device performance is facilitated by introducing pad and interconnect structures, which interconnect the buried BiCMOS devices with top-level pads on InP.

The impact of the additional layers on transistor performance in BiCMOS and InP technologies, respectively,

are shown in Fig. 18 and Fig. 19. Fig. 18 shows the extrapolated transit and maximum oscillation frequencies, respectively, from measurements of BiCMOS transistor devices on completely processed InP-on-BiCMOS wafers. The various curves represent values for devices across a 3-inch wafer area. The horizontal lines in Fig. 18 indicate the maximum values for the transit and maximum oscillation frequencies for devices before heterogeneous integration. These results employ low-loss interconnect via technology. It can be concluded from the figure that the impact of the heterogeneous integration can be estimated to cause a decrease in both values of only around 5 GHz and is not limited by the interconnects.

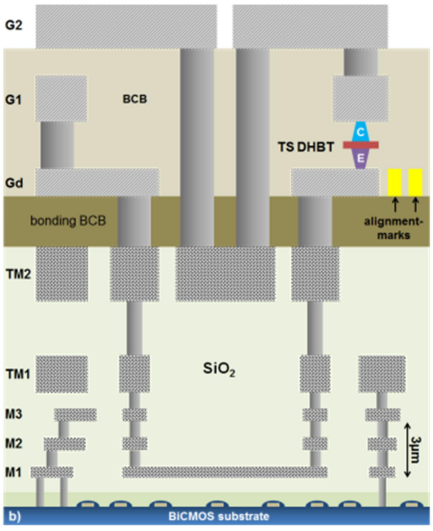

Fig. 17: Cross-section of the InP-on-BiCMOS substrate transfer process. The interconnects between TM2 with G2 and Gd with M1, respectively, form a thin-film microstrip interconnection. Top-level pads are on metal level G2 [9].

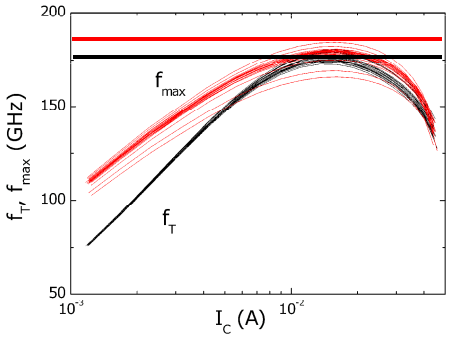

Fig. 18: Interpolated transit frequency f_T and maximum oscillator frequency f_{max} as a function of collector current I_c measured at 30 GHz and an emitter-collector voltage V_{ce} = 1.5 V for eight NPN HBTs in parallel. Horizontal lines indicate the respective values before heterogeneous integration [9].

It has been shown in [10] that device small-signal and large-signal performance of the BiCMOS and InP HBT devices, respectively, remains essentially unaffected by the hetero-integration InP-on-BiCMOS process. Small-signal measurements provided in Fig. 19 indicate that there is only a minor impact by fillers and thermal vias in SiGe BiCMOS on InP DHBT performance. This is most probably due to the fact that the filler structures, as well as the thermal via structures are small and non-interconnected, which has been confirmed by 3D EM simulations.

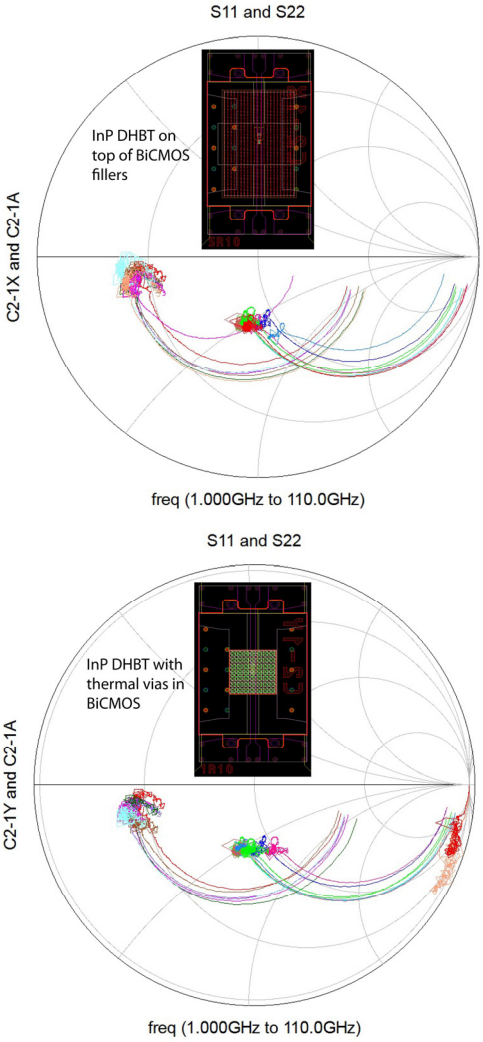

Fig. 19: Small-signal input and output S-parameters of single-finger InP DHBT in a transferred-substrate (TS) process and the same device with fillers in the InP-on-BiCMOS process (top) and implementing a heat-sink underneath the transistor in SiGe (bottom). Measurements are in the range 1 GHz–110 GHz. Cyan and blue lines are results for the standard TS process, red and magenta are results for InP HBT transistors in InP-on-BiCMOS process. Insets show the transistor layout for the two cases, respectively [10].

These results are important for circuit integration in both technologies, which requires dissipation of thermal energy from the top-level InP DHBT devices operating under large-signal conditions.

VI. Summary

It is shown that mm-wave and sub-mm-wave on-wafer characterization presents a challenge from calibration, on-wafer measurement, measurement system and circuit design point of view. The methodologies to overcome these challenges include modified calibration standards avoiding probe coupling and coupling between structures in on-wafer calibration substrates.

These also include the suppression of multi-mode propagation using thin-film transmission lines, as well as appropriate transitions between the levels. The suggestions discussed in the paper lead to improved calibration standards suitable for TRL and LRM calibration methodologies.

It is further shown, that successful attempts exist for small-signal characterization of devices and MMICs up to sub-mm-wave frequencies using thin-film transmission lines. The impact of standard calibration procedures on device characterization is discussed. It is shown that accurate device characterization is important for the verification of the extracted models. Finally, characterization results for heterogeneously integrated devices and MMIC are presented.

ACKNOWLEDGMENT

Viktor Krozer thanks Oerlikon AG for partial financial support.

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